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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,327	03/31/2004	Stephan C. Burdick	15436.250.38	5332

22913 7590 03/23/2007

WORKMAN NYDEGGER
(F/K/A WORKMAN NYDEGGER & SEELEY)
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

EXAMINER	
DUPUIS, DEREK L	
ART UNIT	**PAPER NUMBER**
2883	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,327	BURDICK ET AL.	
	Examiner	Art Unit	
	Derek L. Dupuis	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *9-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I in the reply filed on 12/28/2006 is acknowledged. The traversal is on the ground(s) that claims 20-23 are drawn to a method rather than to a coupling member. The method claims 20-23 are closely related to the product of Group 1. This is found persuasive and therefore claims 20-23 will be examined with the elected group.

The requirement is made FINAL.

2. Claims 9-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12/28/2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Dair et al (US 2002/0028048 A1)*** in view of ***Bartur et al (US 2002/0027689 A1)***.

5. Regarding claim 1, Dair et al teach a system configured to minimize EMI in an optical transceiver. The system includes an optical subassembly (110, 111), a transceiver substrate (205), and a coupling member (106, 108) that communicatively couples the optical subassembly (110, 111) to the transceiver substrate (205). The coupling member (106, 108) comprises a signal trace layer that provides one or more signal pathways (113, 117) between the optical

subassembly (110, 111) and the transceiver substrate (205). The coupling member (106, 108) also includes one or more ground plane layers (114, 118) that connect a body of the optical subassembly (110, 111) to ground. Dair et al do not explicitly teach that the grounding connection is made via a common mode grounding capacitor.

6. Bartur et al teach a transceiver system for reduced noise interference. Bartur et al teach that using a circuit including a grounding capacitor (320 and 314) to reduce common mode noise. See paragraphs 42, 43, and 58.

7. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the transceiver system of Dair et al to include a circuit with a grounding capacitor to reduce common mode noise. Motivation would be the improvement of common mode noise rejection (see paragraph 42 of Bartur et al).

8. Regarding claim 2, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 1. Dair et al teach that the subassembly includes transmitter optical subassembly (110).

9. Regarding claim 3, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 2. Dair et al teach that the subassembly includes transmitter optical subassembly (111).

10. Regarding claim 4, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 1. Dair et al teach that the signal trace layer includes traces that are connected to a laser source (see paragraph 79).

11. Regarding claim 5, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 1. Dair et al teach that the ground plane layer (114, 118) provides EMI

shielding (see paragraphs 5 and 79). It is routine and common in the art to use copper as the metal of ground plates.

12. Regarding claim 6, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 1. Transceivers commonly use operational speeds in the range of 2.5 gigabit, 4.0 gigabit, and 10 gigabits.

13. Regarding claim 7, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 1. Dair et al teach that signal coupling capacitors can be integrated into the device (see paragraph 79) in "in" or "out" paths of the circuitry.

14. Regarding claim 8, Dair et al in view of Bartur et al teach a system as discussed above in reference to claim 7. Dair et al teach that the optical source is a laser diode (see paragraph 79).

15. Regarding claim 20, Dair et al teach a method of minimizing EMI in an optical transceiver. The method includes transferring high-frequency electrical signals between a transceiver substrate (205) and an optical subassembly (110, 111) through a multilayer coupling member (106, 108). The coupling member (106, 108) comprises a signal trace layer that provides one or more signal pathways (113, 117) between the optical subassembly (110, 111) and the transceiver substrate (205). The coupling member (106, 108) also includes one or more ground plane layers (114, 118) that connect a body of the optical subassembly (110, 111) to ground. Dair et al do not explicitly teach that the grounding connection is made via a common mode grounding capacitor.

16. Bartur et al teach a transceiver system for reduced noise interference. Bartur et al teach that using a circuit including a grounding capacitor (320 and 314) to reduce common mode noise. See paragraphs 42, 43, and 58.

17. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the method of Dair et al to use a circuit with a grounding capacitor to reduce common mode noise. Motivation would be the improvement of common mode noise rejection (see paragraph 42 of Bartur et al).

18. Regarding claim 21, Dair et al in view of Bartur et al teach a method as discussed above in reference to claim 20. Dair teaches that the coupling member (106, 108) also includes one or more ground plane layers (114, 118) that connect a body of the optical subassembly (110, 111) to ground to shield EMI (see paragraphs 5 and 79).

19. Regarding claim 22, Dair et al in view of Bartur et al teach a method as discussed above in reference to claim 21. The ground plane layer is attached to a PCB which is an thin insulating material with electrical traces.

20. Regarding claim 23, Dair et al in view of Bartur et al teach a method as discussed above in reference to claim 22. Dair et al teach that signal coupling capacitors can be integrated into the device and connected to the signal trace layers of the coupling member (see paragraph 79).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derek L. Dupuis whose telephone number is (571) 272-3101. The examiner can normally be reached on Monday - Friday 8:30am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Derek L. Dupuis
Group Art Unit 2883

Frank G. Font
Supervisory Patent Examiner
Technology Center 2800